CLAIMS

1. Flexible rate matching apparatus, comprising:

a) a dual shift register (14) having
a1) a configurable data shift register (26) adapted to receive a continuous stream of data items at a prespecified rate of a clock signal; and
a2) a configurable validity shift register (28) adapted to store, for each data item stored in the data shift register (26), an associated indication of validity, and adapted to shift the indications of validity at said prespecified rate;

b) a control unit (12) adapted to modify the contents of the data shift register (26) and the validity shift register (28) through puncturing/ repetition operations so as to achieve a rate matching; and

c) an output handler (16) adapted to output valid data items at said prespecified rate using the indications of validity stored in the validity shift register (28).

2. Flexible rate matching apparatus according to claim 1, wherein said data shift register (26) is adapted to receive a plurality of data items in each cycle of said clock signal.

3. Flexible rate matching apparatus according to claim 1 or 2, wherein the control unit (12) comprises:

a) an input and RM control unit (22) adapted to control said dual shift register (14);

b) an output control unit (23) adapted to control said output handler (16); and

c) a flexible RM control unit (24) adapted to coordinate and synchronize the operations of said input and RM control unit (22) and said output control unit (23).

4. Flexible rate matching apparatus according to one of the claims 1-3, wherein the control unit (12) further comprises a computation unit adapted to determine positions where data items have to be rate-matched according to a rate matching scheme.

5. Flexible rate matching apparatus according to one of the claims 1-4, wherein said puncturing operations include assigning a value indicating non-validity to those indications of validity associated with data items to be punctured.

6. Flexible rate matching apparatus according to one of the claims 1-5, wherein said repetition operations include shifting the data items to be repeated as well as their associated indications of validity to at least two memory locations of the data shift register (26) and the validity shift register (28),

respectively.

7. Flexible rate matching apparatus according to one of the claims 1-6, wherein the output handler (16) is adapted to continuously output data items, where the associated indications of validity stored in the validity shift register (28) have a value indicating validity.

8. Flexible rate matching apparatus according to one of the claims 1-7, characterized in that it has a cascade structure.

9. Flexible rate matching method, comprising the steps of:

a) receiving a continuous stream of data items at a prespecified rate of a clock signal in a configurable data shift register (26);

b) storing, for each data item stored in the data shift register (26), an associated indication of validity in a configurable validity shift register (28) and shifting the indications of validity at said prespecified rate;

c) modifying the contents of the data shift register (26) and the validity shift register (28) through puncture/repetition operations so as to achieve a rate matching; and

d) outputting valid data items at said prespecified rate using said indications of validity stored in the validity shift register (28).

10. Flexible rate matching method according to claim 9, wherein a plurality of data items is received in the data shift register (26) in each cycle of said clock signal.

11. Flexible rate matching method according to one of the claims 9-10, further comprising a step of determining positions where data items have to be rate-matched according to a rate matching scheme.

12. Flexible rate matching method according to one of the claims 9-11, wherein said puncturing operations include assigning a value indicating non-validity to those indications of validity associated with data items to be punctured.

13. Flexible rate matching method according to one of the claims 9-12, wherein said repetition operations include shifting the data items to be repeated as well as their associated indications of validity to at least two memory locations of the data shift register (26) and the validity shift register (28), respectively.

14. Flexible rate matching method according to one of the claims 9-13, wherein said step of outputting valid data items comprises continuously outputting data items where the associated indications of

validity stored in the validity shift register (28) have a value indicating validity.

15. A computer program product directly loadable into the internal memory of a mobile communication unit, comprising software code portions for performing the steps of one of the claims 9 to 14, when the product is run on a processor of the mobile communication unit.

16. A processor program product stored on a processor usable medium and provided for flexible rate matching, comprising:

a) a processor readable program means for causing a processor (22,23,24) to control reception of a continuous stream of data items at a pre-specified rate by a configurable data shift register (26);

b) a processor readable program means for causing the processor (22,23,24) to store, for each data item stored in the data shift register (26), an associated indication of validity in a configurable validity shift register (28);

c) a processor readable program means for causing a processor (22,23,24) to modify the contents of the data shift register (26) and the validity shift register (28) through puncture/ repetition operations so as to achieve a rate matching; and

d) a processor readable program means for causing a processor (22,23,24) to output valid data items at the prespecified clock rate using the indications of validity stored in the validity shift register (28).

17. Flexible rate matching apparatus according to one of the claims 1-4, wherein said puncturing operations include shifting the data items to be punctured as well as their associated indications of validity to no memory location of the data shift register (26) and the validity shift register (28), respectively.

18. Flexible rate matching apparatus according to one of the claims 1-4 and 17, wherein said repetition operations include shifting the data items to be repeated as well as their associated indications of validity to two memory locations of the data shift register (26) and the validity shift register (28), respectively.

19. Flexible rate matching apparatus according to one of the claims 1-4 and 17-18, wherein the output handler (16) is adapted to output data items, where the associated indications of validity stored in the validity shift register (28) have a value indicating validity.

20. Flexible rate matching apparatus according to one of the claims 1-4 and 17-19, wherein said dual shift register (14) includes at least two pipeline stages

each having a different number of memory locations.

21. Flexible rate matching apparatus according to one of the claims 1-4 and 17-20, characterized in that it has a cascade structure.

22. Flexible rate matching method according to one of the claims 9-11, wherein said puncturing operations include shifting the data items to be punctured as well as their associated indications of validity to no memory location of the data shift register (26) and the validity shift register (28), respectively.

23. Flexible rate matching method according to one of the claims 9-11 and 22, wherein said repetition operations include shifting the data items to be repeated as well as their associated indications of validity to two memory locations of the data shift register (26) and the validity shift register (28), respectively.

24. Flexible rate matching method according to one of the claims 9-11 and 22-23, wherein said step of outputting valid data items comprises outputting data items where the associated indications of validity stored in the validity shift register (28) have a value indicating validity.

25. Flexible rate matching method according to one of the claims 9-11 and 22-24, wherein said dual shift register (14) includes at least two pipeline stages

each having a different number of memory locations.

26. A computer program product directly loadable into the internal memory of a communication unit, comprising software code portions for performing the steps of one of the claims 9-14 and 22-25, when the product is run on a processor of the communication unit.